IN THE TITLE:

Please replace the original title with the following title.

--PROCESS FOR FORMING A LOW RESISTIVITY TITANIUM SILICIDE LAYER ON A SILICON SEMICONDUCTOR SUBSTRATE--

IN THE CLAIMS:

Please amend claims 1, 7, 8, 15, and 17-19, and add new claims 30-35 as follows:

1. (Amended) A method for forming a low resistivity titanium silicide layer on a surface of a doped region of a silicon semiconductor substrate, said method comprising the steps of:

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depositing a titanium layer on the surface of the doped region of the silicon semiconductor substrate, the doped region being an n-type or p-type source or drain region;

introducing an effective amount of a metallic element at the interface between the titanium layer and the doped region of the silicon semiconductor substrate so as to promote titanium silicide transformation from C49 phase to C54 phase during a subsequent rapid thermal annealing, the metallic element being chosen from the group consisting of indium, gallium, tin, and lead; and

after the introducing step, performing a rapid thermal annealing of the silicon semiconductor substrate to form titanium silicide.

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7. (Amended) The method as defined in claim 1, wherein the introducing step includes the sub-step of depositing the effective amount of the metallic element on the surface of the doped region of the silicon semiconductor substrate.

8. (Amended) The method as defined in claim 1, wherein the introducing step includes the sub-step of implanting the effective amount of the metallic element into the doped region of the silicon semiconductor substrate.

15. (Amended) A method for fabricating a semiconductor device, said method comprising the steps of:

depositing a titanium layer on the surface of at least one n-type or p-type doped region of a silicon semiconductor substrate;

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introducing an effective amount of a metallic element at the interface between the titanium layer and the at least one doped region of the silicon semiconductor substrate so as to promote titanium silicide transformation from C49 phase to C54 phase during a subsequent rapid thermal annealing, the metallic element being chosen from the group consisting of indium, gallium, tin, and lead; and

after the introducing step, performing a rapid thermal annealing of the silicon semiconductor substrate to form a low resistivity titanium silicide layer.

17. (Amended) The method as defined in claim 15, wherein the effective amount of the metallic element is 1×10^{13} to 5×10^{14} atoms/cm^2.

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18. (Amended) The method as defined in claim 15, wherein the introducing step includes the sub-step of depositing the effective amount of the metallic element on the surface of the at least one doped region of the silicon semiconductor substrate.

19. (Amended) The method as defined in claim 15, wherein the introducing step includes the sub-step of implanting the effective amount of the metallic element into the at least one doped region of the silicon semiconductor substrate.

Please add new claims 30-35 as follows:

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--30. (New) The method as defined in claim 1, wherein the doped region is an n-type region.--

--31. (New) The method as defined in claim 1, wherein the doped region is doped with arsenic.--

--32. (New) The method as defined in claim 1, wherein the metallic element is chosen from the group consisting of gallium, tin, and lead.--

--33. (New) The method as defined in claim 15, wherein the at least one doped region includes at least one n-type source or drain region.--

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--34. (New) The method as defined in claim 15, wherein the at least one doped region includes at least one region doped with arsenic.--

--35. (New) A method for forming a low resistivity titanium silicide layer on a surface of a silicon semiconductor substrate, said method comprising the steps of:

depositing a titanium layer on the surface of the silicon semiconductor substrate;

introducing an effective amount of a metallic element at the interface between the titanium layer and the silicon semiconductor substrate so as to promote titanium silicide transformation from C49 phase to C54 phase during a subsequent rapid thermal annealing, the metallic element being chosen from the group consisting of indium, gallium, tin, and lead; and

after the introducing step, performing a single rapid thermal annealing of the silicon semiconductor substrate to form C54 phase titanium silicide, the metallic element promoting titanium silicide transformation from C49 phase to C54 phase during the single rapid thermal annealing.--